General Description

The MAX9370/MAX9371/MAX9372 LVTTL/TTL-to-differential LVPECL/PECL translators are designed for high-speed communication signal and clock driver applications. The MAX9370/MAX9372 are dual LVTTL/TTL-to-LVPECL/PECL translators that operate in excess of 1GHz. The MAX9371 is a single translator. The MAX9370/MAX9371 operate over a wide 3.0V to 5.25V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. The MAX9372 is designed to operate from 3.0V to 3.6V.

The devices default to output high if the input is disconnected. They feature low 270ps propagation delay. The MAX9370/MAX9371/MAX9372 employ industry-standard flow-through pinouts. These devices are specified for operation from -40°C to +85°C, and are offered in space-saving, 8-pin SOT23, µMAX, and SO packages.

Applications

- Precision Clock/Data Level Translation
- Central Office Clock Distribution
- DSLAM/DLC
- Base Station
- Mass Storage

Features

- Guaranteed 1GHz Operating Frequency at 600mV Differential Output
- 270ps Propagation Delay
- 10ps Output-to-Output Skew (MAX9370/MAX9372)
- Wide Supply Range: 3.0V to 5.25V (MAX9370/MAX9371)
- ESD Protection > 2kV (Human Body Model)
- Output High with Input Open
- Available in Small 8-Pin SOT23, µMAX, and SO Packages
- Improved Upgrades to MC100EL22, MC100EPT20, MC100EPT22

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX9370</td>
<td>-40°C to +85°C</td>
<td>8 SOT23-8</td>
</tr>
<tr>
<td>MAX9370EUA*</td>
<td>-40°C to +85°C</td>
<td>8 µMAX</td>
</tr>
<tr>
<td>MAX9370ESA</td>
<td>-40°C to +85°C</td>
<td>8 SO</td>
</tr>
<tr>
<td>MAX9371</td>
<td>-40°C to +85°C</td>
<td>8 SOT23-8</td>
</tr>
<tr>
<td>MAX9371EUA*</td>
<td>-40°C to +85°C</td>
<td>8 µMAX</td>
</tr>
<tr>
<td>MAX9371ESA</td>
<td>-40°C to +85°C</td>
<td>8 SO</td>
</tr>
<tr>
<td>MAX9372</td>
<td>-40°C to +85°C</td>
<td>8 SOT23-8</td>
</tr>
<tr>
<td>MAX9372EUA*</td>
<td>-40°C to +85°C</td>
<td>8 µMAX</td>
</tr>
<tr>
<td>MAX9372ESA</td>
<td>-40°C to +85°C</td>
<td>8 SO</td>
</tr>
</tbody>
</table>

*Future product—contact factory for availability.

Pin Configurations/Functional Diagrams appears at end of data sheet.

Typical Operating Circuit

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.
ABSOLUTE MAXIMUM RATINGS

VCC to GND (MAX9370/MAX9371) .................-0.3V to +5.5V
VCC to GND (MAX9372).................................-0.3V to +4.0V
D_ to GND ..................................................-0.3V to (VCC + 0.3V)
Q_, Q_ to GND ...........................................-0.3V to (VCC + 0.3V)
Continuous Output Current ................................................50mA
Surge Output Current........................................................100mA
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin SOT23..............................................................+112°C/W
8-Pin µMAX.............................................................+221°C/W
8-Pin SO ............................................................+170°C/W
Junction-to-Ambient Thermal Resistance with
500LFPm Airflow
8-Pin SOT23..............................................................+78°C/W
8-Pin µMAX.............................................................+155°C/W
8-Pin SO ............................................................+99°C/W
Continuous Power Dissipation (TA = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C)............470mW
8-Pin µMAX (derate 4.5mW/°C above +70°C).........362mW
8-Pin SOT23 (derate 8.9mW/°C above +70°C).......714mW
Operating Temperature Range .........................-40°C to +85°C
Junction Temperature ..................................................+150°C
Storage Temperature Range .............................-60°C to +150°C
Soldering Temperature (10s).................................-60°C to +150°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = 3.0V to 5.25V for MAX9370/MAX9371, VCC = 3.0V to 3.6V for MAX9372, outputs terminated with 50Ω ±1% to VCC - 2.0V. Typical values are at VCC = 3.3V, VIH = 2.4V, VIL = 0.4V, unless otherwise noted.) (Notes 1, 2, 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td></td>
</tr>
</tbody>
</table>

LVTTL INPUTS (D_)

Input High Voltage
Vih
2.0 2.0 2.0 2.0 2.0 2.0 V

Input Low Voltage
Vil
0.8 0.8 0.8 0.8 0.8 V

Input Low Current
IIL
VD = 0.5V
-100 -100 -100 -100 -100 µA

Input High Current
IIH
VD = VCC, MAX9370/ MAX9371
130 130 130 130 130 µA
VD = VCC, MAX9372
20 20 20 20 20

Input Clamp Voltage
IIL or IIH = 18mA
-1.2 -1.2 -1.2 -1.2 -1.2 V

LVPECL/PECL OUTPUTS (Q_, Q_)

Output High Voltage
Voh
MAX9370
Vcc - 1.085
Vcc - 1.025
Vcc - 1.025
Vcc - 0.895
Vcc - 0.895

MAX9371/ MAX9372
Vcc - 1.145
Vcc - 1.145
Vcc - 1.145
Vcc - 0.895
Vcc - 0.895

Output Low Voltage
Vol
MAX9370
Vcc - 1.83
Vcc - 1.81
Vcc - 1.81
Vcc - 1.62
Vcc - 1.62

MAX9371/ MAX9372
Vcc - 1.945
Vcc - 1.945
Vcc - 1.945
Vcc - 1.695
Vcc - 1.695

MAXIM
# LVTTL/TTL-to-Differential LVPECL/PECL Translators

**DC ELECTRICAL CHARACTERISTICS (continued)**

(\(V_{CC} = 3.0\text{V to 5.25V for MAX9370/MAX9371, } V_{CC} = 3.0\text{V to 3.6V for MAX9372, outputs terminated with 50\Omega \pm 1\% to } V_{CC} - 2.0\text{V. Typical values are at } V_{CC} = 3.3\text{V, } V_{IH} = 2.4\text{V, } V_{IL} = 0.4\text{V, unless otherwise noted.}) (Notes 1, 2, 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Output Swing ((V_{OH} - V_{OL}))</td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
</tbody>
</table>

**SUPPLY CURRENT**

<table>
<thead>
<tr>
<th>Power-Supply Current (Note 4)</th>
<th>(I_{CC})</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX9370/MAX9372</td>
<td>18</td>
</tr>
<tr>
<td>MAX9371</td>
<td>9.5</td>
</tr>
</tbody>
</table>

**AC ELECTRICAL CHARACTERISTICS**

(\(V_{CC} = 3.0\text{V to 5.25V for MAX9370/MAX9371, } V_{CC} = 3.0\text{V to 3.6V for MAX9372, outputs terminated with 50\Omega \pm 1\% to } V_{CC} - 2.0\text{V, input frequency} \leq 1.0\text{GHz, input transition time} = 125\text{ps} (20\% \text{ to } 80\%), V_{IH} = 2.0\text{V, } V_{IL} = 0.8\text{V. Typical values are at } V_{CC} = 3.3\text{V, } V_{IH} = 2.4\text{V, } V_{IL} = 0.4\text{V, unless otherwise noted.}) (Note 5)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Toggle Frequency</td>
<td>(f_{MAX})</td>
<td>(V_{OH} - V_{OL} \geq 600\text{mV})</td>
<td>1.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>Input-to-Output Propagation Delay</td>
<td>(t_{PLH}, t_{PHL})</td>
<td>Figure 1</td>
<td>200</td>
<td>270</td>
<td>400</td>
</tr>
<tr>
<td>Output-to-Output Skew</td>
<td>(t_{SKQQ})</td>
<td>MAX9370/MAX9372 (Note 6)</td>
<td>10</td>
<td>50</td>
<td>7</td>
</tr>
<tr>
<td>Output Rise/Fall Time</td>
<td>(t_{R}, t_{F})</td>
<td>Figure 1</td>
<td>80</td>
<td>250</td>
<td>80</td>
</tr>
<tr>
<td>Added Deterministic Jitter</td>
<td>(t_{DJ})</td>
<td>1Gbps 2(^{23}) - 1 PRBS pattern (Note 7)</td>
<td>40</td>
<td>60</td>
<td>40</td>
</tr>
<tr>
<td>Added Random Jitter</td>
<td>(t_{RJ})</td>
<td>1GHz clock (Note 7)</td>
<td>0.23</td>
<td>0.8</td>
<td>0.23</td>
</tr>
</tbody>
</table>

**Note 1:** Measurements are made with the device in thermal equilibrium.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** DC parameters are production tested at \(T_A = +25^\circ\text{C. DC limits are guaranteed by design and characterization over the full operating temperature range.}

**Note 4:** All pins are open except \(V_{CC}\) and \(GND\).

**Note 5:** Guaranteed by design and characterization. Limits are set to \(\pm 6\ \sigma\).

**Note 6:** Measured between outputs of the same part at the signal crossing points under identical conditions for a same-edge transition.

**Note 7:** Device jitter added to the input signal.
LVTTL/TTL-to-Differential LVPECL/PECL Translators

**Typical Operating Characteristics**

(MAX9371, VCC = 3.3V, VIH = 2.4V, VIL = 0.4V, outputs terminated with 50Ω to VCC - 2V, input transition time = 125ps (20% to 80%), TA = +25°C, unless otherwise noted.)
LVTTL/TTL-to-Differential LVPECL/PECL Translators

Detailed Description

The MAX9370/MAX9371/MAX9372 LVTTL/TTL-to-differential LVPECL/PECL translators are designed for high-speed communication signal and clock driver applications. The MAX9370/MAX9372 are dual LVTTL-to-LVPECL/PECL translators that operate in excess of 1GHz. The MAX9371 is a single translator. The MAX9370/MAX9371 operate over a wide 3.0V to 5.25V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. The MAX9372 is optimized for 3.0V to 3.6V operation. These devices feature low 270ps propagation delay and 40ps peak-to-peak deterministic jitter.

Inputs and Outputs

The MAX9370/MAX9371/MAX9372 inputs accept standard LVTTL/TTL levels. The input has pullup circuitry that drives the outputs to a differential high if the inputs are open. The outputs are differential LVPECL/PECL levels.

Output Termination

Terminate outputs with 50Ω to VCC - 2V or use an equivalent Thevenin termination. Use the same terminate on each output for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q is used as a single-ended output, terminate both Q and Q̅.

Applications Information

Pin Description for the MAX9370/MAX9372

<table>
<thead>
<tr>
<th>PIN</th>
<th>SO μMAX</th>
<th>SOT23</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td></td>
<td>Q0</td>
<td>Noninverting Differential LVPECL/PECL Output 0. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>2</td>
<td>7</td>
<td></td>
<td>Q̅0</td>
<td>Inverting Differential LVPECL/PECL Output 0. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td></td>
<td>Q1</td>
<td>Noninverting Differential LVPECL/PECL Output 1. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td></td>
<td>Q̅1</td>
<td>Inverting Differential LVPECL/PECL Output 1. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td></td>
<td>GND</td>
<td>Ground. Provide a low-impedance connection to ground plane.</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td></td>
<td>D1</td>
<td>LVTTL/TTL Input 1. LVTTL/TTL input for translator corresponding to output Q1 and Q̅1.</td>
</tr>
<tr>
<td>7</td>
<td>3</td>
<td></td>
<td>D0</td>
<td>LVTTL/TTL Input 0. LVTTL/TTL input for translator corresponding to output Q0 and Q̅0.</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td></td>
<td>VCC</td>
<td>Positive Supply Voltage. Bypass VCC to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.</td>
</tr>
</tbody>
</table>

Pin Description for the MAX9371

<table>
<thead>
<tr>
<th>PIN</th>
<th>SO μMAX</th>
<th>SOT23</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4, 6</td>
<td>4, 5, 8</td>
<td></td>
<td>N.C.</td>
<td>No Connection. No internal connection.</td>
</tr>
<tr>
<td>2</td>
<td>7</td>
<td></td>
<td>Q</td>
<td>Noninverting Differential LVPECL/PECL Output. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td></td>
<td>Q̅</td>
<td>Inverting Differential LVPECL/PECL Output. Typically terminate with 50Ω resistor to VCC - 2V.</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td></td>
<td>GND</td>
<td>Ground. Provide a low-impedance connection to ground plane.</td>
</tr>
<tr>
<td>7</td>
<td>3</td>
<td></td>
<td>D</td>
<td>LVTTL/TTL Input</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td></td>
<td>VCC</td>
<td>Positive Supply Voltage. Bypass VCC to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.</td>
</tr>
</tbody>
</table>
**LVTTL/TTL-to-Differential LVPECL/PECL Translators**

Ensure that the output currents do not exceed the continuous safe output current limit or surge output current limit as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device’s total thermal limits should be observed.

**Supply Bypassing**

Bypass VCC to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel and as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance.

**PC Board Traces**

Input and output trace characteristics affect the performance of the MAX9370/MAX9371/MAX9372. Connect each differential output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

**Chip Information**

TRANSISTOR COUNT: 358  
PROCESS: Bipolar
LVTTL/TTL-to-Differential LVPECL/PECL Translators

Pin Configurations/Functional Diagrams

MAX9370/MAX9371/MAX9372

SO/µMAX

SOT23

VCC

GND

N.C.

Q

D

N.C.

Q

N.C.

VCC

GND

N.C.

Q

D

N.C.

VCC

GND

N.C.

Q

D

N.C.

VCC

GND

N.C.

Q

D

N.C.
LVTTL/TTL-to-Differential LVPECL/PECL Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

NOTE:  
1. ALL DIMENSIONS ARE IN MILLIMETERS.  
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT 
   SURFACE PARALLEL TO DATUM “A.”  
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. 
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING. 
5. EIAJ REF. NUMBER JF-74 (6 LEAD VERSION) 
6. COPLANARITY ± 0.05, MAX. 
7. PIN 1 ID DOT IS 0.3 MM MIN. LOCATED ABOVE PIN 1.  
8. MEETS JEDEC MO-217C.

MAXIM

PACKAGE OUTLINE, SOT-23, 6L

INCHES | MILLIMETERS
--- | ---
A | 0.043 | 1.10
A1 | 0.002 | 0.06
A2 | 0.030 | 0.75
b | 0.010 | 0.25
C | 0.65 | 16.5
D | 0.116 | 2.95
E | 0.116 | 2.95
H | 0.188 | 4.78
L | 0.018 | 0.41
S | 0.007 | 0.18

NOTE:  
1. DUE TO MOLD FLASH, MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006”).  
2. CONTROLLING DIMENSIONS: MILLIMETERS.  
3. MEETS JEDEC MO-217C-6L.

MAXIM

PACKAGE OUTLINE, 8L uMAX/uSOP

INCHES | MILLIMETERS
--- | ---
A | 0.043 | 1.10
A1 | 0.002 | 0.06
A2 | 0.030 | 0.75
b | 0.010 | 0.25
C | 0.65 | 16.5
D | 0.116 | 2.95
E | 0.116 | 2.95
H | 0.188 | 4.78
L | 0.018 | 0.41
S | 0.007 | 0.18

NOTE:  
1. DUE TO MOLD FLASH, MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006”).  
2. CONTROLLING DIMENSIONS: MILLIMETERS.  
3. MEETS JEDEC MO-187C-6L.